HIGH POWER 6-18 GHz H/V SWITCH DESIGNED IN CHANNELIZED WAFER SCALE FABRICATION PROCESS

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Abstract

A 6-18GHz transfer switch is fabricated by a batch process technology, the HMIC (Heterolithic Microwave Integrated Circuit) process using shunt silicon diodes. The fabrication and design utilized a novel transmission medium incorporating signal channelization for high frequency high performance operation.

INTRODUCTION

This paper demonstrates a broadband (6-18 GHz) H/V antenna switch fabricated in a batch process technology that provides insertion loss of 2dB, isolation greater than 35dB, and power handling of more than 8W CW. Batch processing uniformity provides lower reflection coefficient variations as typically required for low radar cross-section.

The high power requirement is satisfied by using only shunt diodes [1,2]. A prototype switch topology is shown in Figure 1 with a filter representing a transmission path shown in Figure 2. The bandwidth of an ideal filter without accounting for the capacitive loading due to the diodes and with no shunt-series arm coupling is 5.2-18.8 GHz with 20dB return loss. A distributed implementation of the above topology has been described previously [2]. While handling more than 6W from 6 to 18GHz, the chip area was larger than desired and isolation suffered from interline coupling. A substantial redesign using extensive shielding and capacitive loading of higher impedance lines with judicious beneficial coupling is described here. A modified filter topology, a new design medium (referred to here as channelized microstrip), and interesting modeling and process technologies were developed to reduce size by a factor of two without performance penalty.

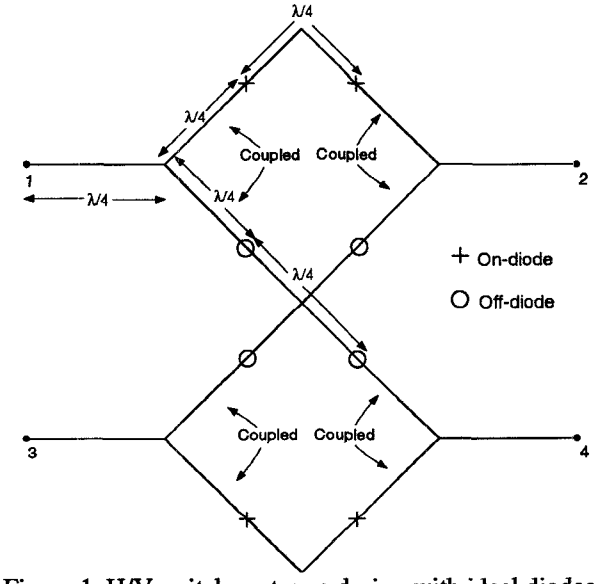

Figure 1. H/V switch protoype design with ideal diodes.

CIRCUIT DESIGN

Previous work [2] demonstrated a switch based on uncoupled shunt and series arms. The topology used there is similar to that illustrated in Figure 1 without the indicated coupling. To further increase the bandwidth of the prototype filter, judicious coupling of the series and shunt legs is incorporated. This coupling increases the bandwidth as the prototype filter now has higher shunt impedance and lower series impedance. Figure 2 shows the return loss of the original and the improved filter with a coupling coefficient of 0.2. It may be seen that the coupling increases the bandwidth by 10%. This filter was used instead of the original filter as it allowed us to incorporate capacitive loading on all transmission lines to reduce the switch size while maintaining the bandwidth.

To increase the isolation to 40dB, a channelized microstrip medium is utilized (microstrip line in an etched channel in silicon). Figure 3 shows the final switch layout and a cross-section illustrating the medium utilized for all transmission line elements. In this way the coupling between various circuit elements was considerably reduced. However, this medium posed major modeling challenges.

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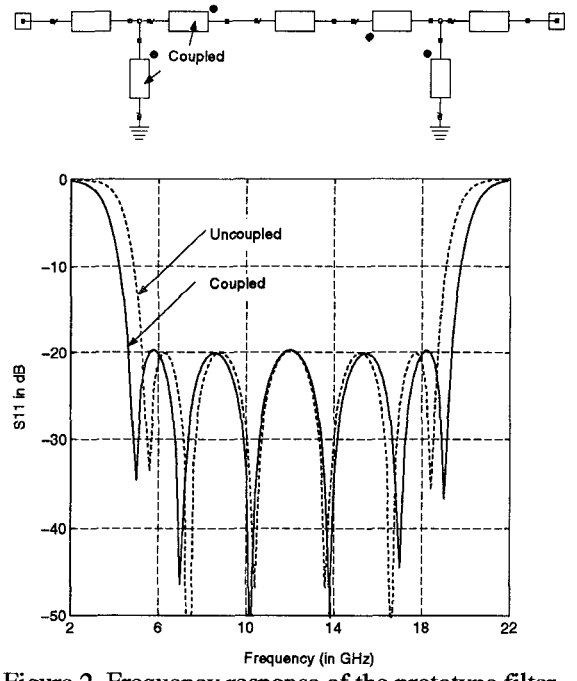

Figure 2. Frequency response of the prototype filter.

SONNET's Em [6] based models were developed to include the sloping side walls (56 degrees dictated by the <111> silicon plane). Since Sonnet is a 2.5D simulator, the inclusion of the side-wall is accomplished by modeling the slope by multiple steps. This technique has been previously demonstrated [6]. The input capacitance loading, and therefore shortening of the first section of the filter, is accomplished with interdigital capacitors. To allow for circuit optimization, the interdigital capacitors are modeled as slow wave structures scalable with the number of sections. The capacitive loading can than be optimized for the best circuit performance. Following the interdigital capacitor is a 400um wide channelized line. This was modeled in SONNET[6] and deembedded externally. Since the bends in the 400um wide line interact, we modeled the two bends together. The connecting line between the bends was varied and again a scalable model was derived. Following the bend is the tapped inductor which proved to be a very complicated structure for EM simulation. To model the tapped inductor we had to split it into two parts; the first part is a 3-port element that has shunt MIM capacitor (used to decrease the switch size) and the second part is a 4 port element that provides the desired coupling to increase the bandwidth. While the first part of the tapped inductor is modeled to be dimensionally scalable with the MIM capacitor length, the second part was initially scalable and then fixed to provide the require coupling of about 0.34. Following the tapped

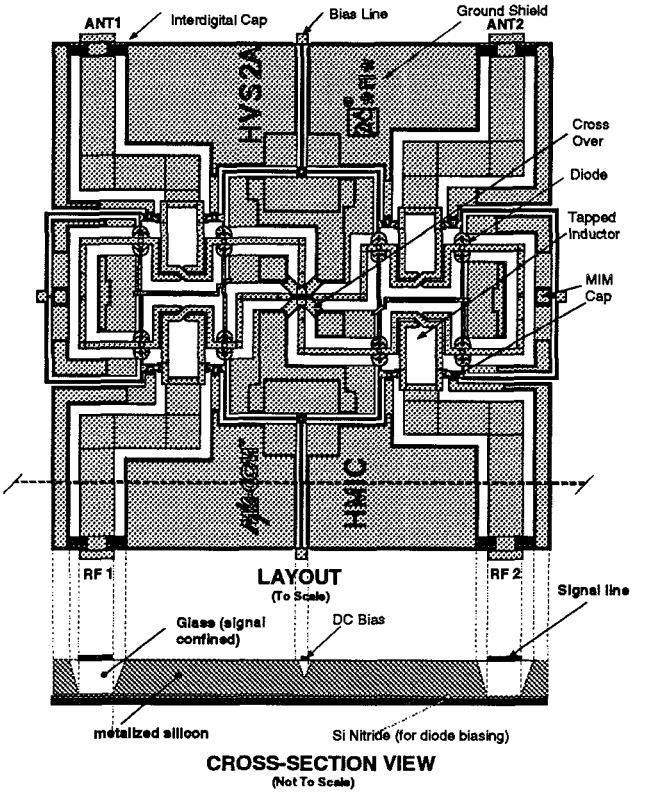

Figure 3. Layout of the channelized switch. Also shown is side-view of a crossection to show the shielding structure. Chip measures 6.3 mm square.

inductors are the HMIC diodes. The diodes are built from an epitaxially grown low-doped Si material in the Silicon pedestal. The diodes have accompanying contact pedestals that bias the diodes at the cathode. The transmission line connects to the anode, which is at the top of the diode [2]. The cathode is isolated from the ground by the intervening layer of SiN providing a 40 pF RF bypass capacitance. Following the diodes are 75um transmission lines that join the transmission lines from the other port. For the path that goes through the center we utilized the already developed crossover, slightly modified to include the shields that follow along the connecting three-mil lines. The switch was modeled in HP-EEsof Libra IV simulator. Various scalable models developed from SONNET simulations were included as subcircuits called by the main circuits.

The selection of the diode is critical for lowest insertion loss. To study the effect of the various process parameters, device physics software from SILVACO was utilized to solve the two-dimensional semiconductor equations. SUPREM4, a module in the SILVACO suite, is used initially to generate the doping profile and the epi structure in the HMIC process. The

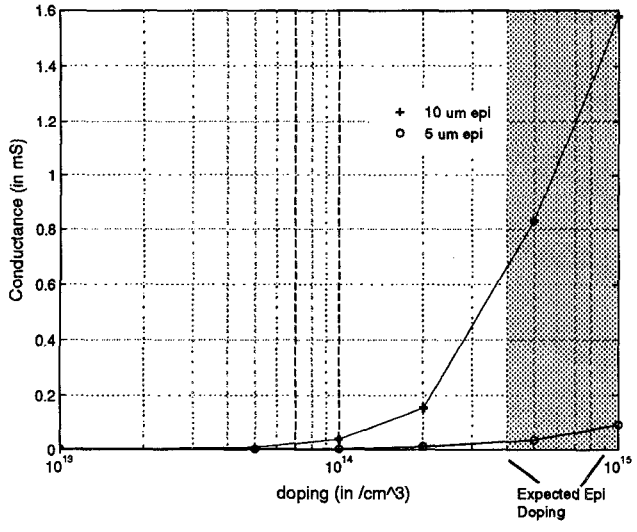

Figure 4. Diode shunt conductance versus doping concentration at 10 V negative bias. The intrinsic capacitance of the diodes is nominally 0.05 pF.

epi layers were then used in another module called SPISCES to generate AC impedances of the diode and from that the conductance at zero and 10V reverse bias. Figure 4 shows the shunt conductance of the diodes for various levels of unintentional background epi layer doping. Typical background doping is in the range of $5x10^{14}$ to $1x10^{15}$ cm^{-3} indicating that 5um epi can give substantially lower shunt conductance. This is apparent because the 5 um epi for the same bias voltage will have higher doping concentrations at the depletion layer edges and therefore lower shunt conductance [8]. The resulting PIN diode I-region thickness from the 5 um epi is about 2.5 um and from the 10um epi about 7.5um, both being sufficient for the required power handling capability as long as sufficient bias voltage is available.

Figure 5 shows the simulated performance for the transmission leg through the crossover. This simulation accounts for the deviation of the diode capacitance from the design value due to an accidental interchange of the 5um mask with the 10um mask. Note that the simulated isolation due to the crossover is better than 35dB.

The layout and the circuit shown in Figure 3 were processed in the HMIC lab at M/A-COM. The process started with highly doped n-type silicon wafers on which the undoped epitaxial layer referred to above was grown. The wafers were then etched to provide cavities which were coated with cobalt and alloyed to form $CoSi_2$ [4]. This highly conductive film forms the RF ground plane. We have found that $CoSi_2$ formed in this manner significantly improves the diode quality and losses. The cavities in the silicon wafers were then filled with glass at about 850°C. Following the glass slumping process, the wafers are polished to within 2-3um from the silicon pedestal. The other top side processes including anode-formation, contact formation, MIM capacitors, air-bridge structures and top metal were then completed. The wafers were coated with photoresist and inverted

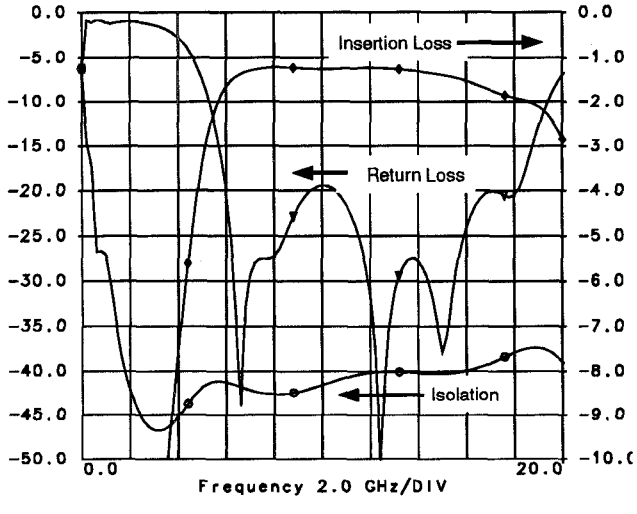

Figure 5. Simulated performance of the cross-under path. The simulated isolation is for the path where the isolation is limited by the cross-over coupling. The other path showed better isolation performance.

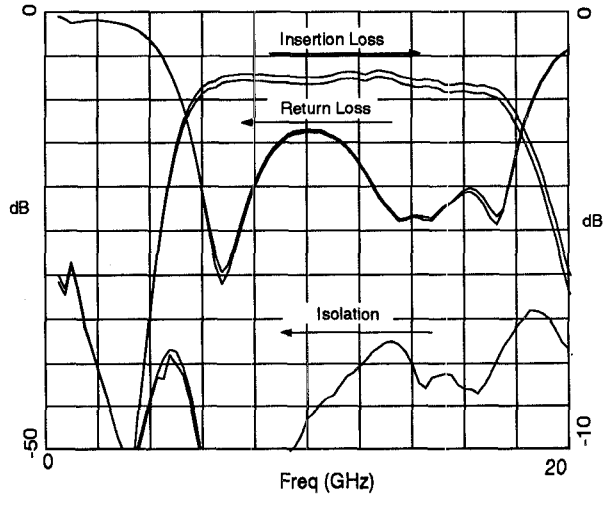

Figure 6. Measured performance of the cross-under path. The measured isolation is for the path where the isolation is limited by the cross-over coupling.

to accomplish the backside processing. The silicon on the backside was first removed and then 0.4um of SiN followed by 2um of gold were deposited. The nitride

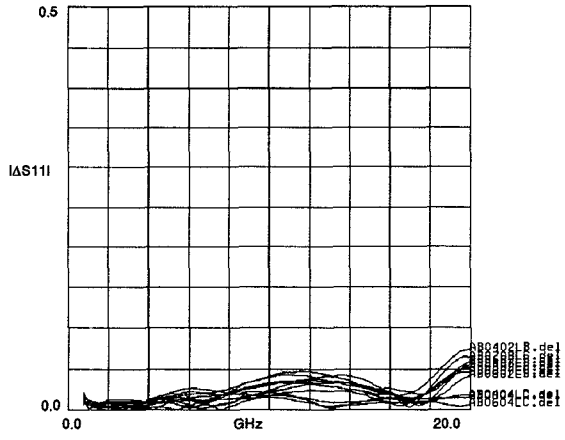

Figure 7. Magnitude of the vector deviation of the measured S_{11} from the mean for the 10 um epi run. The data includes all working paths from three wafers.

provides an RF ground while allowing a DC block for the diodes. For power testing, a test fixture was designed and constructed to provide adequate heat sinking and RF isolation.

RESULTS

Figure 6 shows the measured performance of the switch simulated in Figure 5, displaying close agreement with the measurements. It may be noted that the isolation for the crossover path is more than 35dB across the 6-18GHz band. The isolation for the other path, dictated by the diodes, is more than 45dB. The other paths of the switch behaved similarly, except for the return loss for the side path. The return loss on the side path was as low as 10B at 17GHz probably because of the effect of the bias bypass capacitor close to the RF line.

As expected, the 5um epi provided lower insertion loss by as much as 0.5dB compared with the 10um epi, confirming the SILVACO model predictions.

The RF power testing consisted of ramping the input power from a small signal to several watts for several different bias conditions. During the tests, up to 8W of power was applied to the switch. The switch functioned adequately to 4W input power with -17V bias on the diodes and even higher power can be handled provided adequate bias is provided. Finally, Figure 7 shows that the maximum magnitude of the vector deviation of S_{11} from the mean is less than 0.05 for ten units from three different wafers.

From a limited sample size the measured yield of completely working units is 5%. This low value arises because of the complicated backside processing, the large number of integrated components and immaturity of some of the process steps.

CONCLUSIONS

We have demonstrated a twofold reduction in the switch area from the previous design using EM simulations that utilized a channelized transmission medium and a semi-lumped approach. The previous prototype switch topology was improved by including interline coupling. New processes including cobalt disilicide were used in the fabrication to provide better performance. These improvements gave better isolation in spite of reduced size. Measured data demonstrate low variation of the reflection coefficient between switches from different wafers, an important system consideration. Further work needs to be done to improve the yields of the current process.

Acknowledgments

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References

[1] J. White, Microwave Semiconductor Engineer, Van Nostrand Reinhold Electrical/Computer Engineering Series, NY 1982.

[2] P. Onno, N. Jain, C. Souchuns and J. Goodrich, "High Power 6-18GHz Transfer Switch Using HMIC", 1994 IEEE MTT-S.

[3] J. Goodrich & C. Souchuns, "HMIC - A fully capable Silicon Microwave Integrated Circuit Process", Microwave USA, Tokyo, Sept

[4] M. O'Keefe, N. Jain, & P. Onno, "Low Loss Cobalt Silicide Films for Microwave ICs", Patent Pending.

[5] *SUPREM4 and SPISCES*, SILVACO International Inc., CA, USA.

[6] *Em*, SONNET SOFTWARE Inc., Liverpool, NY, USA.

[7] N. Jain, "Electromagnetic Modeling Using Commercial Electromagnetic Simulators", 1994 IEEE MTT-S Workshop on Electromagnetic Simulations.

[8] H. M. Olson, "Design Calculations of Reverse Bias Characteristics for Microwave p-i-n Diode", IEEE Trans. on Electron Devices, Vol., ED-14, No. 8, Aug. 1967, pp 418-427.